DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY MODULE; the specification of which was filed on March 7, 2002 as U.S. Patent Application No. 10/094,512.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Jayesh R. Bhakta
Inventor's signature fausash R. Bharate.
Date 4-24-02
Residence: 12220 Rose Street, Cerritos, California 90703
Citizenship: United States
Post Office Address: Same as above.
Full name of second inventor: Robert S. Pauley, Jr.
Inventor's signature I what
Date 4-29-02
Residence: 26322 Eastview Court, San Juan Capistrano, California 92675
Citizenship: United States
Post Office Address: Same as above.
Send Correspondence To:

Send Correspondence To: KNOBBE, MARTENS, OLSON & BEAR, LLP Customer No. 20,995 JTS-13599.DOC:ke20020412